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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,320	09/29/2003	Robert M. Ellis	42P17514	4655

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EXAMINER	
SCHNEIDER, JOSHUA D	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,320	ELLIS ET AL.	
	Examiner	Art Unit	
	Joshua D. Schneider	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 6/15/2006 have been fully considered but they are not persuasive. With regards to the arguments to the rejections under 35 USC 102(e), the arguments are not persuasive. The argument to the rejections in view of Walker is based on a narrow reading of the limitations of the claims. All claims are based on the broadest reasonable interpretation of the claims. Applicant was not able to allege any element being missing form the rejection of the claim, but rather argues that the elements shown were not part of a memory device. However, the delineation between where the "memory device" starts and ends is not set forth in the claim in such a way to avoid the rejection, and in fact is only listed as a part of the preamble, which is given no patentable weight. The rejection should therefore be read as the memory device encompassing everything cited by the examiner. All of the elements in Figure 6 can be aptly characterized to together define a memory device despite the fact that they are called by different names in the reference.

2. The arguments to the rejections under 35 USC 103 are persuasive as the references are properly disqualified.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-12 and 17-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. With regards to claim 1, it is unclear how a memory device in the preamble can compromise a memory device (line 4). The language requiring the memory device to encompass itself is confusing and unclear and does not allow one to comprehend what is being claimed. The term memory device cannot logically be used to define a part of a memory device.

6. Claims 2-12 are rejected for incorporating the same indefinite subject matter as the independent claim upon which they depend.

7. Claims 17-27 recite the limitation "memory device" in the preamble. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 2, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,845,472 to Walker et al.

10. With regards to claim 1, Walker teaches a storage array comprised of a plurality of memory cells (column 4, lines 27-45), an interface buffer coupled to the storage array (column 4, lines 41-47, and column 4, lines 12-26), and having a first interface to couple the memory device to a first memory bus to couple the memory device to an external memory controller (Fig. 6, elements 60 or 68), and memory error logic associated with the interface buffer to carry out a check for memory errors within the storage array during a period of time in which there are no

transactions carried out by the external memory controller on the first memory bus that involve the storage array (column 8, lines 46-51).

11. With regards to claim 2, Walker teaches the memory error logic is a component of the interface buffer, and wherein the memory device is comprised of a circuit board to which is attached at least one integrated circuit that comprises the storage array and at least one integrated circuit that comprises the interface buffer (column 5, lines 66, through column 6, lines 29).

12. With regards to claim 11, Walker teaches bus error logic associated with the interface buffer to carry out a check for bus errors in transactions across the first memory bus between the external memory controller and the first interface (column 7, lines 19-33).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 3-10, 12-19, and 21-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,845,472 to Walker et al. in further view of U.S. Patent Application Publication 2002/0167791 to Goris.

15. With regards to claim 3, Walker teaches the first memory bus provides a point-to-point connection between the memory device and the external memory controller (Fig. 6, element 60), but does not teach the interface has a second point-to-point connection. Goris teaches the interface buffer has a second interface to couple the memory device to a second memory bus to provide a point-to-point connection between the memory device and another memory device,

and the interface buffer passes through bus activity between the first and second memory busses that does not involve the storage array (Fig. 7, paragraphs 23-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the error correction system of Walker using the point to point topology of Goris in order to take advantage of the speed increases of point to point topologies over arbitrated topologies.

16. With regards to claim 13, Walker teaches a storage array comprised of a plurality of memory cells (column 4, lines 27-45), an interface buffer coupled to the storage array (column 4, lines 41-47, and column 4, lines 12-26), and having a first interface to couple the memory device to a first memory bus to couple the memory device to an external memory controller (Fig. 6, elements 60 or 68), and memory error logic associated with the interface buffer to carry out a check for memory errors within the storage array during a period of time in which there are no transactions carried out by the external memory controller on the first memory bus that involve the storage array (column 8, lines 46-51) but does not teach the interface has a second point-to-point connection. Goris teaches a local interface to a storage array comprised of a plurality of memory cells; a first interface to couple the storage array to a first memory bus to couple the storage array to an external memory controller wherein the first memory bus provides a point-to-point connection between the first interface and the external memory controller, a second interface to couple the storage array to a second memory bus to couple the second interface to another interface buffer to couple another storage array to the external memory controller through the interface buffer wherein the second memory bus provides a point-to-point connection between the second interface and the other interface buffer (Fig. 7, paragraphs 23-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to

implement the error correction system of Walker using the point to point topology of Goris in order to take advantage of the speed increases of point to point topologies over arbitrated topologies.

17. With regards to claim 27, Walker teaches a processor (column 3, lines 25-35), a disk storage device coupled to the processor a memory controller coupled to the processor (column 3, lines 36-57), a first memory bus coupled to the memory controller (column 3, line 63, through column 4, line 11), a first memory device having a first storage array comprised of a plurality of memory cells and a first interface buffer coupled within the first memory device to the first storage array (column 4, lines 27-45), and first and second memory error logics associated with the interface buffer to carry out a check for memory errors within the storage array during a period of time in which there are no transactions carried out by the external memory controller on the first memory bus that involve the storage array (column 8, lines 46-51), but does not teach the interfaces using a point-to-point topology. Goris teaches the first interface buffer provides a first interface by which the first memory device is coupled to the first memory bus forming a point-to-point connection between the memory controller and the first interface, a second interface, a second memory bus coupled to the second interface; and a second memory device having a second storage array comprised of a plurality of memory cells and a second interface buffer coupled within the second memory device to the second storage array, wherein the second interface buffer provides a third interface by which the second memory device is coupled to the second memory bus forming a point-to-point connection between the third interface and the second interface, (Fig. 7, paragraphs 23-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the error correction system of Walker using

the point to point topology of Goris in order to take advantage of the speed increases of point to point topologies over arbitrated topologies.

18. With regards to claims 4 and 16, Walker does not teach the use of packets, but official notice is given that the use of packets in memory transfers is notoriously well known in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the error correction system of Walker using the notoriously well known use of packets in order to allow the network to transmit longer messages more efficiently and reliably.

19. With regards to claims 5 and 17, Walker teaches the memory error logic monitors activity on the first memory bus to identify a dead time in which no commands are received from the first memory bus involving the storage array (column 8, lines 46-51), providing an opportunity for the memory error logic to proactively carry out a check for a memory error by reading a portion of the storage array and examining the bits that are read for an indication of a memory error without delaying the carrying out of an access command from the external memory controller involving the storage array (column 10, lines 8-40).

20. With regards to claims 6, 18, and 28, Walker teaches the memory error logic proactively carries out a check for a memory error during a period of time in which a transaction between the external memory controller and the other memory device occurs (column 5, lines 66, through column 6, lines 29).

21. With regards to claims 7, 19, 29, and 30, Walker teaches the memory error logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the storage array will be transmitted by the external memory controller (column 8, lines 46-51, and column 10, lines 8-40) by means of a programmable control register (column

10, line 41, through column 11, line 6), providing an opportunity for the memory error logic to proactively carry out a check for a memory error by reading a portion of the storage array and examining the bits that are read for an indication of a memory error without delaying the carrying out of an access command involving the storage array (column 10, lines 8-40).

22. With regards to claims 9 and 21, Walker teaches the memory error logic carries out a check for a memory error during an access operation commanded by the external memory controller to determine if there is an indication of a memory error in bits of data being read from the storage array (column 5, lines 66, through column 6, lines 29).

23. With regards to claims 10 and 22, Walker teaches the memory error logic corrects a memory error, if a memory error is detected and is correctable, and the memory error logic transmits a signal to the memory controller if a memory error is detected and is not correctable (column 6, line 60, through column 7, line 18).

24. With regards to claims 23 and 25, Walker teaches bus error logic associated with the interface buffer to carry out a check for bus errors in transactions across the first memory bus between the external memory controller and the first interface (column 7, lines 19-33).

25. With regards to claims 12, 24, and 26, Walker does not teach the use of CRC, but official notice is given that it is notoriously well known in the art at the time of invention to examine CRC information and bus error logic examining the data and the CRC information to check for an occurrence of a bus error. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the well known CRC checking to implement the error correction system of Walker in order to take advantage of the CRC's abilities detecting common errors caused by noise in transmission channels.

26. With further regards to claims 25 and 26, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the error checking of the first bus on the second and subsequent busses taught by Goris to use the point to point topology of Goris to implement the error correction system of Walker in order to take advantage of the speed increases of point to point topologies over arbitrated topologies.

27. With regards to claim 14, Walker teaches the memory error logic is a component of the interface buffer, and wherein the memory device is comprised of a circuit board to which is attached at least one integrated circuit that comprises the storage array and at least one integrated circuit that comprises the interface buffer (column 5, lines 66, through column 6, lines 29).

28. With regards to claim 15, Walker does not teach, but Goris teaches the first interface is coupled to the first memory bus and the second interface is coupled to the second memory bus when the memory device is coupled to another circuit board to which the external memory controller is attached (Fig. 7, paragraphs 23-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the error correction system of Walker using the point to point topology of Goris to in order to take advantage of the speed increases of point to point topologies over arbitrated topologies.

29. Claims 8, 20, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,845,472 to Walker et al. and U.S. Patent Application Publication 2002/0167791 to Goris in further view of U.S. Patent 6,349,390 to Dell et al.

30. With regards to claims 8, 20, and 31, Walker and Goris fail to teach the powering down of the inactive bus, but Dell teaches the memory error logic monitors the first memory bus for the occurrence of a powering down of the first memory bus, providing an opportunity for the

memory error logic to opportunistically carry out a check for a memory error by reading a portion of the storage array and examining the bits that are read for an indication of a memory error without delaying the carrying out of an access command involving the storage array (powering removed by opening FETs, column 4, lines 1-65). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the power removed error checking of Dell with the combined error correction system of Walker and Goris in order to correct memory errors quickly and without interruption.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua D. Schneider whose telephone number is (571) 272-4158. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDS

KIM HUYNH
SUPERVISORY PATENT EXAMINER
9/1/06